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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/865,006	05/23/2001	Krishna Parat	042390P7462D	4672

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EXAMINER
DIAZ, JOSE R

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/06/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/865,006	PARAT ET AL.	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

➢ The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

➢ Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by Wada et al. (US Patent No. 5,087,584).

Regarding claim 5, Wada et al. teach a method (see cols. 1-12) comprising the steps of: forming a first and second stack (27) on a tunnel oxide (19) and separated by a gap (26) (see Figure 7); forming a shared source region (31, 32) (see Figure 7); forming first and second drain regions (30) (see Figure 7); forming and anisotropically etching a dielectric layer (35) (see Figure 9).

➢ Claim 6 is rejected under 35 U.S.C. 102(e) as being anticipated by Chi et al. (US Patent No. 6,184,084 B1).

Regarding claim 6, Chi et al. teach a method (see cols. 1-10) comprising the steps of: forming a tunnel oxide (42) (see Figure 3A), a first polysilicon film (44) (see Figure 3B), an interpoly dielectric (46) (see Figure 3C) and second polysilicon film (48) (see Figure 3D); polishing said second polysilicon film (see col. 7, lines 26-30); and etching said layers to form a polysilicon/dielectric/polysilicon stack (see Figure 3F).

Claim Rejections - 35 USC § 103

➢ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

➢ Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Witek et al. (US Patent No. 6,146,970) in view of Arghavani et al. (US Patent No. 6,261,925 B1).

Regarding claim 4, Witek et al. teach a process (see cols. 1-14) comprising the steps of: forming a trench (210) (see Figure 6); growing an oxide (212) (see Figure 7); filling said trench with a dielectric (216a) (see Figure 8); growing a tunnel oxide (254) (see Figure 14); forming a first polysilicon layer (260) (see Figure 14); forming an interpoly dielectric (262) (see Figure 14); and forming a polysilicon control gate (264) (see Figure 14). However, Witek et al. fail to teach the steps of growing and removing

an oxide in said trench. Arghavani et al. teach a very well known trench isolation process (see cols. 1-10) wherein an oxide (150) is formed in a trench (145) and then, said oxide is removed from the trench (see Figures 1C-1E). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Witek et al. to include the step of growing and removing an oxide in a trench. The ordinary artisan would have been motivated to modify Witek et al. in the manner described above for at least the purpose of removing debris from the trench sidewalls.

- Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wada et al. (US Patent No. 5,087,584) in view of Wang et al. (US Patent No. 6,312,991 B1).

Regarding claim 7, Wada et al. teach a method (see cols. 1-12) comprising the steps of: forming a first and second stack (27) on a tunnel oxide (19) and separated by a gap (26) (see Figure 7); forming a shared source region (31, 32) (see Figure 7); forming first and second drain regions (30) (see Figure 7); forming and anisotropically etching a BPSG dielectric layer (34) (see Figure 8); and forming a metal silicide (see col. 8, lines 1-5). However, Wada et al. fail to explicitly disclose the steps of forming and heating a metal film in order to form the metal silicide disclosed. Wang et al. teach that it is well known in the art to form a metal silicide layer by forming a metal layer and then, heating said metal layer (see col. 7, lines 8-18). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Wada et al. to include the steps of forming and heating a metal film in order to form a metal silicide. The ordinary artisan would have been motivated to modify Wada et al. in

the manner described above for at least the purpose of providing a lower resistance contact.

Conclusion

➢ The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chen (US Pat. No. 6,277,693 B1) discloses self-aligned process for forming source line of a flash memory device. Cremonesi et al. (US Patent No. 6,180,460 B1) disclose a process for manufacturing a non-volative memory with reduced resistance of the common source lines. Mehrad et al. (US Patent No. 6,071,779) disclose source line fabrication process for flash memory. Mehrad (US Patent No. 6,268,248 B1) discloses method of fabricating a source line in flash memory having STI structures. Ishige (US Patent No. 5,648,285) disclose method for manufacturing semiconductor nonvolatile memory device with field insulating layer. McElroy (US Patent No. 4,373,248) discloses a common source line in Figures 4a-6e.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 8:00 - 5:00 Monday through Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD
November 30, 2001

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800